



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patentee: Deppe, et al. Docket No.: 2004 P 50797 US
Serial No.: 10/815,223 Art Unit: 2818
Filed: March 31, 2004 Examiner: Andy Huynh
Patent No.: 6,972,226 B2 Issue Date: December 6, 2005
For: Charge-Trapping Memory Cell Array and Method for Production

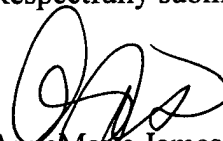
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Date of Deposit: December 29, 2005

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Request for Issuance of Certificate of Correction – Patent (1 page)
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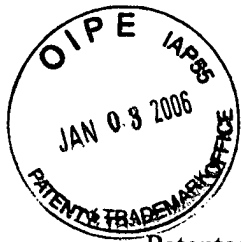
Respectfully submitted,


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Request for Issuance of Certificate of Correction
Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322

Dear Sir:

Upon review of the above-identified issued patent, Patentee notes errors in the claims that should be corrected as shown on Form PTO/SB/44, attached hereto in duplicate.

None of the mistakes noted on the attached Certificate of Correction were incurred through fault of the Patentee, therefore no fee is required.

Patentee respectfully solicits the issuance of the requested Certificate of Correction.

Respectfully submitted,

Ira S. Matsil
Reg. No. 35,272

12/29/05

Date

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. 6,972,226 B2
APPLICATION NO. : 10/815,223
ISSUE DATE : December 6, 2005
INVENTOR(S) : Deppe, et al.

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 7, line 24; delete "part" insert --parts--
Column 8, line 65; delete "sad" insert --said--
Column 8, line 66; delete "her" insert --further--

MAILING ADDRESS OF SENDER(Please do not use customer number below):

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